AMENDMENTS

IN THE CLAIMS:

Please amend claims 1, 4 and 6 as follows below.

1. (Currently amended) An integrated circuit, comprising:

an array of ferroelectric memory cells, each cell having a capacitor stack having a ferroelectric core with a crystallization in the (001) family, ~~the ferroelectric cores having asymmetric domains,~~ wherein at least ~~about~~ 40% of the domains are functionally oriented with respect to the capacitor stack, and wherein at least one of the capacitor stacks comprises a conductive contact formed thereover or thereunder, or both, and wherein the conductive contact has a cross section near a contact portion with the top portion of the stack, the bottom portion of the stack, or both, that is about as large or larger than that of the ferroelectric cores.

2. (Original) The integrated circuit of claim 1, wherein from about 45 to about 75% of the domains are functionally oriented with respect to the capacitor stack.

3. (Original) The integrated circuit of claim 1, wherein the ferroelectric cores are PZT cores and the PZT of each core has a switched polarization of at least about 60 μC/cm2.

4. (Currently amended) The integrated circuit of claim 1, further comprising:

a dielectric layer covering the array of memory cells, the dielectric layer having a ~~metal filled via~~ conductive contact over each ferroelectric core, the ~~vias~~ conductive contacts each having a cross section about as large or larger than that of the ferroelectric cores.

5. (Original) The integrated circuit of claim 1, wherein electrodes adjacent opposing sides of the ferroelectric cores have a collective thickness of at least about 200 nm thick.

6. (Currently amended) The integrated circuit of claim 1, wherein each of the capacitor stacks are formed over ~~metal filled vias~~ conductive contacts, the ~~vias~~ conductive contacts each having a cross section near their top that is about as large or larger than that of the ferroelectric cores.

7. (Withdrawn) A method of manufacturing an integrated circuit, comprising:

forming an array of ferroelectric memory cells on a semiconductor substrate, the ferroelectric memory cells having ferroelectric cores, the ferroelectric cores having a Curie temperature;

bringing the substrate to a temperature near a Curie temperature of the ferroelectric cores.

subjecting the substrate to a temperature program, whereby thermally induced stresses on the ferroelectric cores cause a switched polarization of the cores to increase by at least about 25% as the cores cool to about room temperature.

completing the processing of the substrate without raising the temperature above the Curie temperature.

8. (Withdrawn) The method of claim 7, wherein the ferroelectric cores comprise PZT and the temperature program comprises keeping the ferroelectric cores within about 100 °C of the Curie temperature for at least about 40 minutes.

9. (Withdrawn) The method of claim 7, wherein the ferroelectric cores comprise PZT and the temperature program comprises keeping the ferroelectric cores within about 100 °C of the Curie temperature for at least about 100 minutes.

10. (Withdrawn) The method of claim 7, wherein the ferroelectric cores comprise PZT and the temperature program comprises keeping the ferroelectric cores within about 50 °C of the Curie temperature for at least about 50 minutes.

11. (Withdrawn) The method of claim 7, wherein the ferroelectric cores comprises PZT and are formed at a temperature of at least about 600 °C.

12. (Withdrawn) The method of claim 7, wherein the ferroelectric cores are in capacitor stacks formed over metal filled vias and the vias each have a cross section near their top that is about as large or larger than that of the ferroelectric cores.

13. (Withdrawn) The method of claim 7, wherein over the array of memory cells there is a layer comprising dielectric having a via over each memory cell, the vias being filled with a metal and each via having an area greater than or equal to the area of the ferroelectric core of the underlying memory cell.

14. (Withdrawn) The method of claim 7, wherein an electrode adjacent the ferroelectric cores comprises iridium and is at least about 200 nm thick.

15. (Withdrawn) An integrated circuit, comprising:

an array of ferroelectric memory cells, having ferroelectric cores; and

over the array of memory cells, a layer comprising dielectric having a via over each memory cell, the vias being filled with a metal and each via having an area greater than or equal to the area of the ferroelectric core of the underlying memory cell.

16. (Withdrawn) The integrated circuit of claim 15, wherein electrodes adjacent opposing sides of the ferroelectric cores have a collective thickness of at least about 200 nm thick.

17. (Withdrawn) The integrated circuit of claim 15, wherein the ferroelectric cores are in capacitor stacks formed over metal filled vias, the vias each having a cross section near their top that is about as large or larger than that of the ferroelectric cores.

18. (Withdrawn) The integrated circuit of claim 15, wherein the ferroelectric cores are in capacitor stacks and comprise domains and at least about 40% of the domains are functionally oriented with respect to the capacitor stack.

19. (Withdrawn) The integrated circuit of claim 15, wherein the ferroelectric cores are in capacitor stacks and comprise domains and from about 45 to about 75% of the domains are functionally oriented with respect to the capacitor stack

20. (Withdrawn) The integrated circuit of claim 15, wherein the ferroelectric cores are PZT cores and the PZT of each core has a switched polarization of at least about 60 μC/cm2.